Online Testable Fault Tolerant Full Adder in Reversible Logic Synthesis

Sajib Kumar Mitra, Md. Faisal Hossain, Shahed Anwar and Ahsan Raja Chowdhury

***Abstract*— Irreversibility dissipates energy and drives power hungry technology and more liability goes to recover bit loss. Reversible computing improves bit loss at input through unique mapping to output and also used in low-power CMOS, Quantum computing and Optical computing. But bit error is another concern of power consumption and it would be recovered by using fault tolerant technique in reversible computing. In this paper we propose Fault Tolerant Full Adder with minimum quantum cost and also online testable. Online testability provides run time testing facility to detect bit error whereas Fault Tolerant is able to correct error.**

***Index Terms*— Reversible Computing, Fault Tolerant, Online Testable, Quantum Computing.**

I. Introduction

Reversible Computing is only one method to recover bit loss by using unique mapping between input and output. But Irreversible technology dissipates kT*log2 joules of heat energy to reload per bit loss information which is computed by the author of [1], where k is the Boltzmann's constant and T is the absolute area temperature. Alternatively reversibility disposes of all the undesired intermediate results by retracing the steps of the first stage in backward order and energy dissipation per logical steps is less than kT [2].

In Quantum computing qubits preserve the states of each computation [3], the transformation of genetic code from DNA to messenger RNA in Bioinformatics [2] and information encryption are the various fields of use logical reversibility. Reversible computations have some limitations:

i. Fan-out always equal to one
ii. Feed back is strictly prohibited

Another fact is the number of garbage bits and gates whose have a lower bound to implement the arbitrary output functions [4, 5]. Reversible circuit is able to espouse same parity between input-output bit patterns to provide fault tolerance facility. In this paper, we propose a novel Online Testable Fault Tolerant Full Adder (OTFTFA) which able to perform fast error detection & correction.

Manuscript received November 15, 2010; revised November 30, 2010. The review of this paper was arranged by Convener Dr. Himanshu B. Soni.

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Rest of the paper is organized as follows: Section II discusses about Reversible Logic, Fault Tolerant, Online Testability and Quantum realization of circuit. Section III illustrates the mechanism to combine Fault Tolerant and Online Testability. Section IV describes the design of Online Testable Fault Tolerant full adder. Section V ends with concluding remarks and future plan.

II. Basic Definitions and Properties

Now a day reversible computing is enhanced from various domains like Quantum computing, Nanotechnology and Optical computing etc. Fault Tolerant detects error and also provides correction facilities [6], [9].

A. Reversible Logic

Reversibility ensures unique mapping between input and output bit patterns where unit logic entities are represented as gates.

Let $I_v = (I_1, I_2, \ldots, I_n)$ and $O_v = (O_1, O_2, \ldots, O_n)$ are input and output vectors of a reversible gate, then the relation is $I_v \leftrightarrow O_v$. Many popular gates have been proposed in this literature.

For example, Feynman Gate (FG) [7], Peres Gate (PG) [8], Feynman Double Gate (F2G) [9], Toffoli Gate (TG) [10] and Fredkin Gate (FRG) [11], New Fault Tolerant Gate (NFT) [12] are shown in Fig. 1.

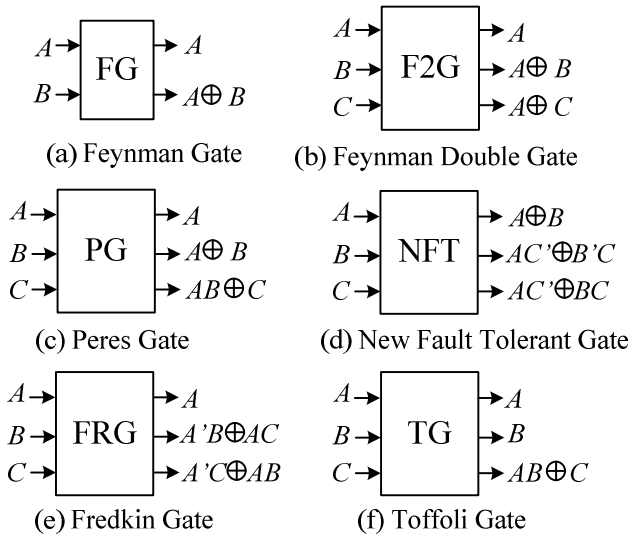

Fig. 1. Reversible Gates with Input-Output mapping

B. Fault Tolerant Method: Parity Preserving

Parity Preserving (PP) is a property of reversible logic where the input and output vectors of a circuit preserves same parity (odd or even). Consider R is a reversible gate has unique

mapping between input and output has to maintain the following constraint to be Fault Tolerant gate:

$$I_1 \oplus I_2 \oplus \cdots \oplus I_n = O_1 \oplus O_2 \oplus \cdots \oplus O_n$$

In Fig. 1 only FRG, F2G and NFT preserve parity and retrain the unique between input-output vectors [12]. Table 1 shows the reversibility and parity preserving of FRG gate.

TABLE I
TRUTH TABLE OF FRG GATE

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Useful Fault Tolerant or Parity Preserving gate is not possible less than 3x3 dimensions [9]. Another Fault Tolerant Gates, IG [13], MIG [14] and Parity Preserving HCG (PPHCG) [6] are 4x4 in Dimension, shown in Fig. 2.

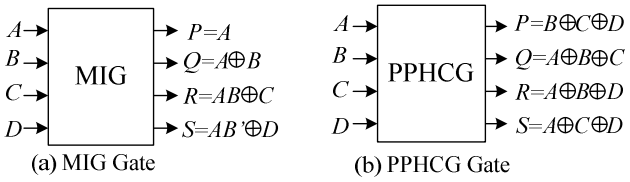

Fig. 2. 4x4 dimensional Fault Tolerant Gates

C. *Built-In Self Testing: Online Testability*

Online Testability uses single output bit to verify alteration of bit at another output lines for a testable gate [15], [17]. An n-dimension reversible gate will be online testable gate if it has following properties [18]:

$$O_n = I_n \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_n$$

In Fig. 3, R1 and R2 both are Online Testable (OT) gates [16]. To detect error the combination of R1, R2 produces cascading block (shown in Fig. 3.c) with two testing Inputs (P, R) and two testing outputs (Q, S) that satisfies following properties:

$$P \oplus R = Q \oplus S$$

The value of Q and S are testing outputs whose combination will be impractical respect to desired one if any bit error occur at another outputs of R1.

Reference [18] used Deduced Reversible Gate (DRG) and Testable Reversible Cell (TRC) which are equivalent to Testable Gate and Testable Cascading Block respectively.

A. *Quantum Realization: Cost Calculation*

Quantum Realization of reversible circuit is another trend to verify circuit performance. Quantum computing uses qubits rather than binary bits and computes multiple operations in a single computation by using matrix operation [3].

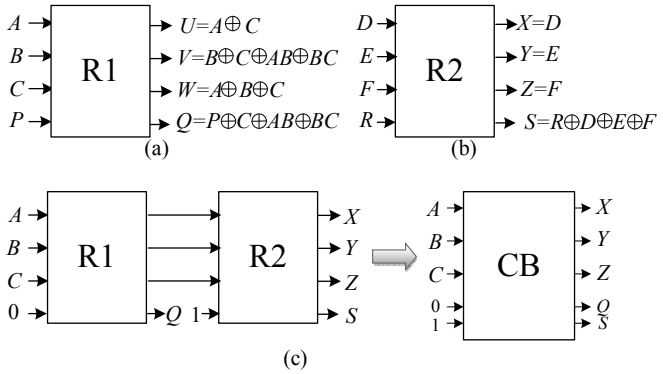

Fig. 3. (a) R1 Testable Gate, (b) R2 Testable Gate and (c) Testable Cascading Block (CB)

Those operations are composed into logical quantum gates which are used to realize reversible circuit. The total number of 2-input quantum gates which are used to realize any circuit is called the Quantum Cost of that circuit. The realization process is done by using bidirectional method [4], [5] which is helpful to minimize gate and garbage cost or computer aided design (CAD) [3]. Reversible XOR operation is equivalent of Controlled-NOT operation of quantum circuit and NOT operation is the multiplication of two pauli – x gate [3] (i.e. V). For that, V is called Square Root of NOT (SRN) gate and V^+ is Hermitian of V that produces $VV^+ = I$ (Identity Matrix). Equivalent quantum circuit of popular reversible gates is shown in Fig. 4.

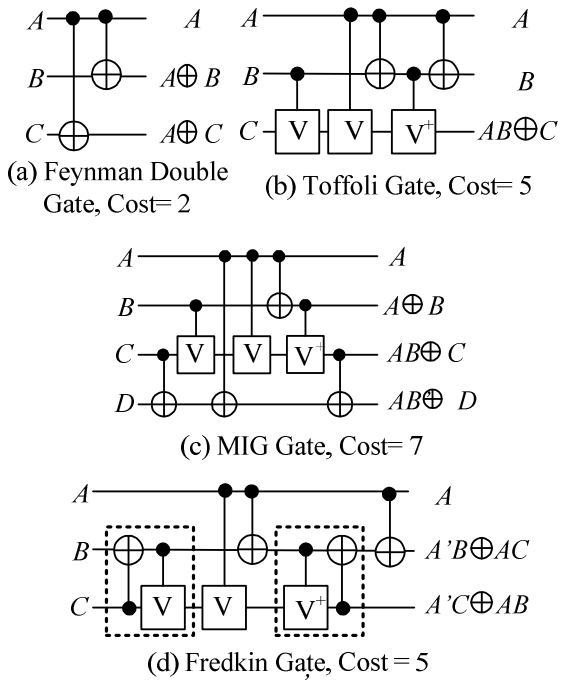

Fig. 4. Quantum realization of Reversible gates

III. Online Testable Fault Tolerant Circuit Design

Online Testing is Built-In Self Testing which detects error where the correction is covered by Fault Tolerant circuit. Any n-dimension reversible gate can be Deduced Reversible Gate (DRG) by adding extra input bit(s) and corresponding output bit(s) [18]. But DRG loses the fault tolerant property due to provide Online Testability.

Theorem 1: Any DRG can never be a Parity Preserving Gate.

Proof: Let, R is a Parity Preserving reversible gate which input and output vectors are $I_v = (I_1, I_2, \ldots, I_n)$ and $O_v = (O_1, O_2, \ldots O_n)$ where $I_v \leftrightarrow O_v$ that maintains the following rule:

$$I_1 \oplus I_2 \oplus \cdots \oplus I_n = O_1 \oplus O_2 \oplus \cdots \oplus O_n \qquad (I)$$

On the other hand, the migration of R into DRG (R_a) can be done by adding extra one input and corresponding output bit.

If we consider both online testability and fault tolerant then R_a has the following properties:

$$I_1 \oplus I_2 \oplus \cdots \oplus I_{n+1} = O_1 \oplus O_2 \oplus \cdots \oplus O_{n+1} \qquad (II)$$

and

$$O_{n+1} = I_{n+1} \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_{n+1} \qquad (III)$$

According to (II) and (III), we get,

$$I_1 \oplus I_2 \oplus \cdots \oplus I_{n+1} = I_{n+1}$$

This is impractical. Hence, R_a can never be a Parity Preserving Gate.

So, any DRG can never be a Fault Tolerant or Parity Preserving Gate. □

But it is possible to build Fault Tolerant Online Testable Reversible Block (CB) [15], [16], [17] which can be produced only from fault tolerant gates.

Theorem 2: Any (*N*x*N*) Parity Preserving Reversible gate can be migrated into a (*N*+2) x (*N*+2) Fault Tolerant Testable Reversible Cell.

Proof: Let R be an NxN Parity Preserving Reversible gate with input-output vectors mapping: $I_v \leftrightarrow O_v$, so the migrated Testable Reversible Cell will justify $I_v (I_1, I_2, \ldots, I_{n+2}) \leftrightarrow O_v (O_1, O_2, \ldots O_{n+2})$ where

$$O_{n+1} = I_{n+1} \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_n \qquad (IV)$$

and

$$O_{n+2} = I_{n+2} \oplus O_1 \oplus O_2 \oplus \cdots \oplus O_n \qquad (V)$$

By Applying XOR operation between (IV) and (V) we get

$$O_{n+1} \oplus O_{n+2} = I_{n+1} \oplus I_{n+2} \qquad (VI)$$

Equation (VI) shows that the testing input and output bits of TRC preserve parity itself.

So (*N*+2) x (*N*+2) Testable Reversible Cell will be Fault Tolerant only if it is generated by (*N* x *N*) parity preserving Gates. □

Finally Deduced Reversible Gates (DRG) can never be Fault Tolerant but corresponding Testable Reversible Cells (TRC) [18] will preserve parity according to above Theorems.

For example, the FRG Generator (FRGG) and FRG Propagator (FRGP) both are equivalent to DRG whose are not fault tolerant but Online Testable (shown in Fig 5(a) and 5(b)). The combination of FRGG and FRGP construct Fault Tolerant Testable Reversible Cell of FRG (FRG TRC) which is shown in Fig. 5.c.

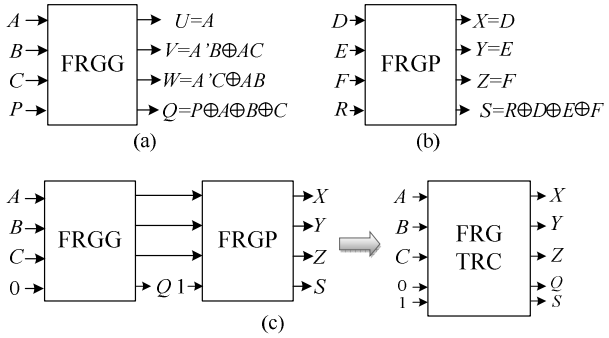

Fig. 5. Fault Tolerant Online Testable Reversible Cell: (a) FRG Generator, (b) FRG Propagator and (c) FRG Testable Reversible Gate

IV. Proposed Design

Full Adder is the most imperative circuit for computation which has three inputs (*A, B, C_{in}*) and the output functions are Sum (*SUM*) and carry (C_{out}) with the following mapping:

$$SUM = A \oplus B \oplus C_{in}$$

$$C_{out} = AB \oplus BC_{in} \oplus AC_{in}$$

Next algorithm is proposed to build a Fault Tolerant Full Adder (shown in Fig. 6) with minimum quantum cost by using minimum dimensional fault tolerant gates which is easily adoptable into minimum dimension of Online Testable Block.

Algorithm 1: Construction_of_ Fault_Tolerant_Full_Adder

Input : *A, B, C_{in}.*
Output: *SUM, C_{out}*
Begin
1. Generate (*A*⊕*B*) by F2G gate
2. Make two copies of C_{in} by another F2G gate
3. Propagate (*A*⊕*B*) and generate C_{out} by FRG using C_{in}
4. Generate Sum by XORing (*A*⊕*B*) with C_{in} by final F2G.

End

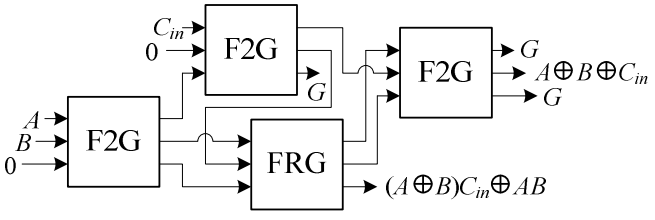

Fig. 6. Proposed Fault Tolerant Reversible Full Adder Circuit

It is better to realize circuit using minimum dimensional reversible gate. Greater dimension causes huge quantum cost. The Online Testable version of the above circuit including Fault Tolerant feature is shown in Fig. 7. Table 2 shows the comparative performance with existing proposed circuit according to quantum cost. Following algorithm describes the construction methodology of Online Testable Fault Tolerant Full Adder.

Algorithm 2: Online_Testable_Fault_Tolerant_FullAdder

Input : A, B and C_{in}
Output: $SUM = (A \oplus B \oplus C_{in})$ and $C_{out} = (AB \oplus BC \oplus CA)$
Begin

1. Adopt all required 3x3 reversible F2G and FRG gates into 5x5 TRC.
2. Set testing input of every TRCs as complement (one is 0 and another is 1) all Testable Blocks.
3. Set connection according to Algorithm (1) which generates C_{out} from FRG TRC and sum from final F2G TRC.

End

V. CONCLUSION

Reversible logic is an emerging research area. In this paper we have presented the design of Fault Tolerant Online Testable Full Adder with minimum dimensional Fault Tolerant gates. Our proposed Fault Tolerant Full adder also has minimum Quantum cost which is one 11. Another property of the proposed design is: Carry generation takes delay is only two and that methodology will enhance the design of Fast Reversible Fault Tolerant Online Testable Adder. Finally, we have described an efficient approach to merge both Online Testing and Fault Tolerant mechanism in a single module as well as we proposed minimum cost Online Testable Fault Tolerant Full Adder in reversible logic synthesis. This mechanism will be used to design Fault Tolerant Online Testable Reversible Carry Look Ahead (CLA) adder and Carry Skip Adder (CSA) in future which will be more reliable to detect and correct error.

TABLE II
COMPARISON BETWEEN PROPOSED AND EXISTING FAULT TOLERANT FULL ADDER CIRCUIT

Fault Tolerant Full Adder	Total Gates		Total Garbage	Quantum Cost
	3x3	4x4		
Proposed	4	0	3	11
Existing[14]	0	2	3	14
Existing[19]	6	0	6	18
Existing[20]	4	0	3	20

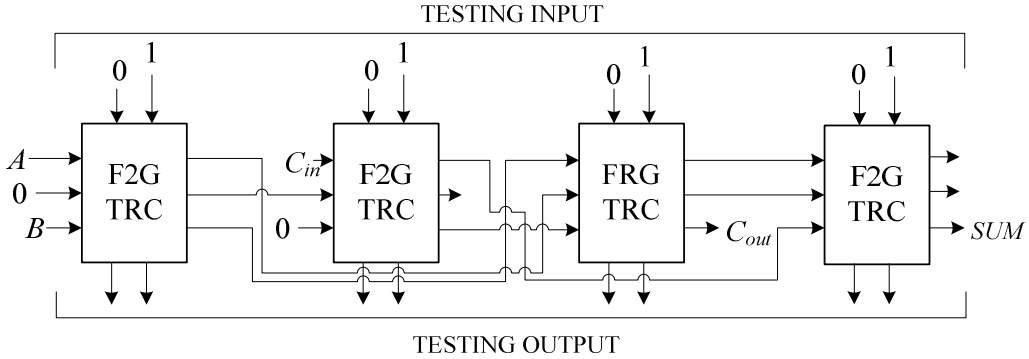

Fig. 7. Proposed Design of Online Testable Fault Tolerant Full Adder

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